If you are using a printed copy of this procedure, and not the on-screen version, then you <u>MUST</u> make sure the dates at the bottom of the printed copy and the on-screen version match.

The on-screen version of the Collider-Accelerator Department Procedure is the Official Version.

Hard copies of all signed, official, C-A Operating Procedures are available by contacting the

ESSHQ Procedures Coordinator, Bldg. 911A

C-A OPERATIONS PROCEDURES MANUAL

ATTACHMENT

4.120.124.a.1 ATF Critical Device - 1 Tests

OPM Procedures in which this Attachment is used.			
4.120.124			

Hand Processed Changes

HPC No.	<u>Date</u>	Page Nos.	<u>Initials</u>	
	Approved:	Signature on File		
		Physics Department Chair		Date

4.120.124.a.1 ATF Critical Device - 1 Tests

PASS ANNUAL ACCEPTANCE TEST PROTOCOL

Division A Software Filename and Checksum: Title:	Checksum:
Division B Software Filename and Checksum: Title:	Checksum:
Initial testing complete:	
Test Team Leader's Name (Print):	Life Number:
Test Team Leader's Name (Sign):	Date:/
Acceptance test procedure complete (following repairs and retesting if required):	
Test Team Leader's Name (Print):	Life Number:
Test Team Leader's Name (Sign):	Date://
Test results reviewed by:	
Safety Section Head's Name (Print):	Life Number:
Safety Section Head's Name (Sign):	Date:/
Test results accepted by Radiation Safety Committee:	
RSC Member's Name (Print):	Life Number:
RSC Member's Name (Sign):	Date:/

1.1 Test for conditions required for Beamline Shutter (BS) to be in Open position

	VERIFY	BS is	CLOSED
	VERIFY VERIFY	Attempt to open BS in ATF Control Room (ACR) User interlock, encl 5809 Connr P9, Pins 1&2 Shorted	FAIL OK
	VERIFY	Attempt to open BS in ATF Control Room (ACR)	FAIL
	SWEEP	Experimental Hall (EH)	
	VERIFY	EH is	SWEPT
	VERIFY	Attempt to open BS in ATF Control Room (ACR) encl 5811	FAIL
	INSERT VERIFY	ACR Permit #1 Key #25 in switch in ACR encl 5811and capture Attempt to open BS in ATF Control Room (ACR)	FAIL
	INSERT	ACR Permit #2 Key #26 in switch in ACR encl 5811and capture	
	VERIFY	Attempt to open BS in ATF Control Room (ACR)	FAIL
	INSERT	Beam Line Lock Out (BLLO) left key #28 in switch in encl 5809 and	
	VERIFY	capture BS enable light at encl 5811	ON
	VERIFY	Attempt to open BS in ATF Control Room (ACR)	SUCCESSFUL
	, 23441 I	recompeted open 25 m rrrr Condor Room (reck)	5000255102
	CLOSE	BS at encl 5811 in ACR	
	VERIFY	BS	CLOSED
	OPEN VERIFY	BS at encl 5811 in ACR BS	OPEN
	VERIF I	D S	OFEN
	TURN	Door A release at encl 5811 in ACR	
	VERIFY	BS	CLOSED
	VERIFY	RIA 🗆 and RIB 🗆	TRIP
	RESTORE	Door A release PLA with SOP leavend PLA Poset	
	RESET VERIFY	RIA with SOR key and RIA Reset RIA	RESET
	OPEN	BS	
	VERIFY	BS	OPEN
	VERIFY	Attempt to Reset RIB with SOR key and RIB Reset	FAIL
	INSERT	Beam Line Lock Out (BLLO) right key #27 in switch in encl 5809	
	VERIFY	and capture Attempt to Reset RIB with SOR key and RIB Reset	FAIL
	VERIFY	At encl 5809 RIBL light is	OFF
	TURN	RIB Test key in encl 5809	
	VERIFY	At encl 5809 RIBL light is	ON
	VERIFY	Attempt to Reset RIB with SOR key and RIB Reset	SUCCESSFUL
	TURN	Door B release at encl 5811 in ACR	
	VERIFY	BS	CLOSED
	VERIFY	RIA	TRIP
	RESTORE	Door B release	
_	RESET	RIA with SOR key and RIA Reset	DECET
	VERIFY OPEN	RIA BS	RESET
	VERIFY	BS BS	OPEN
	TURN	Permit #1 key at encl 5811 in ACR	CI OCET
	VERIFY	BS RIA	CLOSED
	VERIFY RESTORE	Permit #1 key	TRIP
	RESET	RIA with SOR key and RIA Reset	
			5

	VERIFY	RIA	RESET
	OPEN	BS	
	VERIFY	BS	OPEN
	TURN	Permit #2 key at encl 5811 in ACR	
	VERIFY	BS	CLOSED
	VERIFY	RIA	TRIP
	RESTORE	Permit #2 key	
	RESET	RIA with SOR key and RIA Reset	
	VERIFY	RIA	RESET
	OPEN	BS	
	VERIFY	BS	OPEN
	TELEDAT	I . C. DI I O I	
_	TURN	Left BLLO key at encl 5809 BS	CLOSED
	VERIFY VERIFY	RIA	TRIP
	RESTORE	Left BLLO key	IMI
	RESET	RIA with SOR key and RIA Reset	
	VERIFY	RIA	RESET
Ш	OPEN	BS	KESE I
	VERIFY	BS	OPEN
	,		0121
	VERIFY	Attempt to open Door A with Keypad	UNSUCCESSFUL
	OPEN	Double Door C with ATF 15 key	
	VERIFY	EH Sweep	DROPS
	VERIFY	BS	CLOSED
_	Y/EDIEY/	Attached to a serial December 1	CHOOFCOFII
	VERIFY	Attempt to open Door A with Keypad	SUCCESSFUL
	Check for a position	cceptance of Test for conditions required for Beamline Shutter (BS) t	o be in Open

1.2 Test to verify conditions for Modulators to be Enabled ON

VERIFY	1KW Linac □ and Gun □ Amplifiers	LOTO
REMOVE VERIFY	LOTO from Modulators 1 & 2 (Mod 1 \square & Mod 2 \square) Mod 1 \square & Mod 2 \square are	NO LOTO
VERIFY VERIFY VERIFY VERIFY	Mod1 □ & Mod2 □ are Attempt to Enable On Mod1 □ and Mod2 □ EH is BS is Linac tunnel	ENABLED OFF FAIL NOT SWEPT CLOSED
SWEEP VERIFY VERIFY VERIFY	Linac tunnel is MS A □ (right side) and MS B □ (left side)are At Mezz. Encl 5812, Mezz Interlock Box (MIB): RIA □, RIB □, Exptl Hall Interlock (EHI) A □, EHI B □, RIA#1 □ and RIB#2 □ are	SWEPT CLOSED ON
VERIFY VERIFY VERIFY SWEEP	At encl 5813 , Mod1 Contactor Box (M-1CB), RIA \square and RIB \square are At encl 5814 , Mod2 Contactor Box (M-2CB), RIA \square and RIB \square are Attempt to Enable On Mod1 \square and Mod2 \square	ON ON SUCCESSFUL
VERIFY OPEN	EH is BS	SWEPT
VERIFY VERIFY	BS is Mod1 □ and Mod2 □ are still	OPEN ENABLED ON
OPEN VERIFY VERIFY VERIFY VERIFY	MS A at Linac Plug Door MS A is At Mezz. Encl 5812, MIB: RIA □, EHI A □ and RIA#1 □ are At encl 5813, M-1CB, RIA □ and encl 5814, M-2CB, RIA □ are At encl 5813 Mod1 □ and at encl 5814 Mod2 □ are Attempt to Enable On Mod1 □ and Mod2 □	OPEN OFF OFF ENABLED OFF FAIL
CLOSE VERIFY VERIFY VERIFY	MS A At Mezz. Encl 5812 , MIB : RIA □, EHI A □ and RIA#1 □ are At encl 5813 , M-1CB , RIA □ and encl 5814 , M-2CB , RIA □ are Attempt to Enable On Mod1 □ and Mod2 □	ON ON SUCCESSFUL
OPEN VERIFY VERIFY VERIFY VERIFY	MS B at Linac Plug Door MS B is At Mezz. Encl 5812, MIB: RIB □, EHI B □ and RIB#2 □ are At encl 5813, M-1CB, RIB □ and encl 5814, M-2CB, RIB □ are At encl 5813 Mod1 □ and at encl 5814 Mod2 □ are Attempt to Enable On Mod1 □ and Mod2 □	OPEN OFF OFF ENABLED OFF FAIL
CLOSE VERIFY VERIFY VERIFY	MS B At Mezz. Encl 5812 , MIB : RIB □, EHI B □ and RIB#2 □ are At encl 5813 , M-1CB , RIB □ and encl 5814 , M-2CB , RIB □ are Attempt to Enable On Mod1 □ and Mod2 □	ON ON SUCCESSFUL
OPEN	Door A of EH with release at ACR and hold open	
VERIFY VERIFY VERIFY	At Mezz. Encl 5812 , MIB : RIA \square , EHI A \square and RIA#1 \square are At encl 5813 , M-1CB , RIA \square and encl 5814 , M-2CB , RIA \square are BS	OFF OFF CLOSED

	VERIFY VERIFY RESET	At encl 5813 Mod1 □ and at encl 5814 Mod2 □ are Attempt to Enable On Mod1 □ and Mod2 □ RIA at encl 5809 with SOR key	ENABLED OFF FAIL
	VERIFY	RIA is	RESET
	VERIFY	At Mezz. Encl 5812 , MIB : RIA □, EHI A □ and RIA#1 □ are	ON
	VERIFY	At encl 5813 , M-1CB , RIA □ and encl 5814 , M-2CB , RIA □ are	ON
	VERIFY	Attempt to Enable On Mod1 □ and Mod2 □	SUCCESSFUL
_	CLOSE VERIFY	Door A of EH Door A of EH	CLOSED
	VERIFY	Mod1 □ and Mod2 □ are still	ENABLED ON
	DISABLE	Mod1 □ and Mod2 □	
	VERIFY	Mod1 □ and Mod2 □ are	ENABLED OFF
	Check for	acceptance of Test to verify conditions for Modulators to be Enal	bled ON
		Primary Critical Device Response with the ATF Chicane Magnet 1 and 2 Turned On and Pulsing	in the ON state and
	VERIFY	CMSK is set to	ON
	VERIFY	On Detls Pge ACR sees Key SW ON: Div A \square and Div B \square	ON
Ш	VERIT I	Oil Delis I ge ACR sees Rey SW ON. Div A \(\) and Div B \(\)	OIT
	VERIFY TURN ON	ACR sees voltages for: CM1 □, CM2 □, CM3 □ and CM4 □ are Power Supply for Chicane Magnets in Run mode	$0 \pm .5 \text{ V}$
	VERIFY	ACR sees voltages for: CM1 \square , CM2 \square , CM3 \square and CM4 \square are	~ 2.35 V
	VERIFY	ACR sees CDEV_1	Enabled OUT
	VERIFY	ACR sees RHK_DV1 \square and RHK_DV2 \square are	Enabled OFF
	VERIFY	ACR sees Reachback	OK
	VERIFY	ACR sees on Detls pge CDEV_1: Div A □ and Div B □	Enabled OUT
	VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A	Enabled OFF
	VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B	Enabled OFF
	VERIFY	Exp Hall (EH) \square and ATF Linac (AL) \square are	SWEPT
	VERIFY TURN ON	Mod 1 \square and Mod 2 \square Arc Interlock Statuses (AIS) are 208V to Mod 1 and Mod 2	OK
	VERIFY	208V to Mod 1 □ and Mod 2 □ are	ON
	VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A	Enabled ON
	VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B	Enabled ON
	TURN ON	HV to Mod 1 and Mod 2	
	VERIFY	HV to Mod 1 \square and Mod 2 \square are	ON
	Р&Н	At encl 5805, ACMRA, Div A S1 for >10 secs	
	VERIFY	ACR sees on Detls pge >10% Fault, Div A	FAULT
	VERIFY	ACR sees on Detls pge CDEV_1: Div A	Disabled IN
	VERIFY	ACR sees on Detls pge CDEV_1: Div B	Enabled IN
	P&H	At encl 5806, CIB, Div A Laser Shutter Test button for > 2secs	
	VERIFY VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B	Disabled OFF Enabled OFF

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	VERIFY VERIFY	ACR sees Reachback Div A Audio Alarm	Fault OFF
	VERIFY VERIFY	Mod 1 □ and Mod 2 □ are Mod 1 □ and Mod 2 □ AIS are	OFF FAULT
	VERIFY VERIFY VERIFY	Attempt to Turn On 208V to Mod 1 □ and Mod 2 □ Attempt to Turn On HV to Mod 1 □ and Mod 2 □ Attempt to Reset Mod 1 □ and Mod 2 □ Ready Light	FAIL FAIL OK
	VERIFY VERIFY	Attempt to Reset >10% fault Attempt to Reset Reachback	SUCCESSFUL SUCCESSFUL
_ _ _	VERIFY VERIFY VERIFY	ACR sees on Detls pge CDEV_1: Div A □ and Div B □ ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B	Enabled OUT Enabled OFF Enabled OFF
	VERIFY VERIFY	ACR sees CDEV_1 ACR sees RHK_DV1 □ and RHK_DV2 □ are	Enabled OUT Enabled OFF
	TURN ON VERIFY	208V to Mod 1 and Mod 2 208V to Mod 1 \square and Mod 2 \square are	ON
	VERIFY VERIFY	Attempt to Reset Mod 1 \square and Mod 2 \square AIS Mod 1 \square and Mod 2 \square AIS are	SUCCESSFUL OK
	VERIFY VERIFY TURN ON VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B HV to Mod 1 and Mod 2 □ are	Enabled ON Enabled ON ON
	P&H VERIFY VERIFY VERIFY	At encl 5805, ACMRA, Div B S2 for >10 secs ACR sees on Detls pge >10% Fault, Div B ACR sees on Detls pge CDEV_1: Div A ACR sees on Detls pge CDEV_1: Div B	FAULT Enabled IN Disabled IN
	Р&Н	At encl 5806, CIB, Div B Laser Shutter Test button for > 2secs	
	VERIFY VERIFY VERIFY VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B ACR sees Reachback Div B Audio Alarm	Enabled OFF Disabled OFF Fault OFF
	VERIFY VERIFY	Mod 1 □ and Mod 2 □ are Mod 1 □ and Mod 2 □ AIS are	OFF FAULT
	VERIFY VERIFY VERIFY	Attempt to Turn On 208V to Mod 1 □ and Mod 2 □ Attempt to Turn On HV to Mod 1 □ and Mod 2 □ Attempt to Reset Mod 1 □ and Mod 2 □ AIS	FAIL FAIL FAIL
	VERIFY VERIFY	Attempt to Reset >10% fault Attempt to Reset Reachback	SUCCESSFUL SUCCESSFUL
	VERIFY	ACR sees on Detls pge CDEV_1: Div A \square and Div B \square	Enabled OUT

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	VERIFY VERIFY	ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B	Enabled ON Enabled ON		
	VERIFY VERIFY	ACR sees CDEV_1 ACR sees RHK_DV1 □ and RHK_DV2 □ are	Enabled OUT Enabled ON		
	VERIFY VERIFY	Attempt to Reset Mod 1 □ and Mod 2 □ AIS Mod 1 □ and Mod 2 □ AIS are	SUCCESSFUL OK		
	TURN ON VERIFY VERIFY VERIFY TURN ON	208V to Mod 1 and Mod 2 208V to Mod 1 □ and Mod 2 □ are ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div A ACR sees on Detls pge RHK_DV1 □ and RHK_DV2 □, Div B HV to Mod 1 and Mod 2	ON Enabled ON Enabled ON		
	VERIFY	HV to $Mod 1 \square$ and $Mod 2 \square$ are	ON		
	Turn OFF VERIFY Turn OFF VERIFY	HV to Mod 1 and Mod 2 HV to Mod 1 □ and Mod 2 □ are 208V to Mod 1 and Mod 2 208V to Mod 1 □ and Mod 2 □ are	OFF OFF		
	☐ Check for acceptance of Test of Div A Incorrect Primary Critical Device Response with the ATF Chicane Magnet in the ON state and the Modulators 1 and 2 turned On.				
Т	est interlocks	will turn off Modulators while Turned ON and Pulsing			
	LOTO VERIFY	1KW Linac and Gun Amplifiers 1KW Linac □ and Gun □ Amplifiers	L ОТО		

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□ VERIFY 1KW Linac □ and Gun □ Amplifiers LOTO □ VERIFY LOTO is removed from Modulators 1 & 2 (Mod1 □ & Mod2 □) □ VERIFY Mod1 □ & Mod2 □ are ENABLED O □ VERIFY Attempt to Enable On Mod1 □ and Mod2 □ FAIL □ VERIFY EH is NOT SWEPT □ VERIFY BS is CLOSED	
□ VERIFY Mod1 □ & Mod2 □ are ENABLED O □ VERIFY Attempt to Enable On Mod1 □ and Mod2 □ FAIL □ VERIFY EH is NOT SWEPT	
□ VERIFY Attempt to Enable On Mod1 □ and Mod2 □ FAIL □ VERIFY EH is NOT SWEPT	
□ VERIFY EH is NOT SWEPT	FF
□ VERIFY EH is NOT SWEPT	
□ VERIFY RS is CLOSED	
SWEEP Linac tunnel	
□ VERIFY Linac tunnel is SWEPT	
\Box VERIFY MS A \Box (right side) and MS B \Box (left side) are CLOSED	
□ VERIFY At Mezz. Encl 5812, Mezz Interlock Box (MIB): RIA □, RIB □,	
Exptl Hall Interlock (EHI) $A \square$, EHI $B \square$, RIA#1 \square and RIB#2 \square ON	
are	
□ VERIFY At encl 5813, Mod1 Contactor Box (M-1CB), RIA □ and RIB □ ON	
are	
□ VERIFY At encl 5813, Mod2 Contactor Box (M-2CB), RIA □ and RIB □ ON	
are	
\square VERIFY Attempt to Enable On Mod1 \square and Mod2 \square SUCCESSFU	L
SWEEP EH	
□ VERIFY EH is SWEPT	
OPEN BS	
□ VERIFY BS is OPEN	
□ VERIFY Mod1 □ and Mod2 □ are still ENABLED O	N
TURN ON Low Voltage to Mod1and Mod2	
□ VERIFY Low Voltage to Mod1 □ and Mod2 □ are ON	
TURN ON High Voltage to Mod1and Mod2	

VERIFY	High Voltage to Mod1 \square and Mod2 \square are	ON
OPEN VERIFY VERIFY VERIFY VERIFY VERIFY VERIFY	MS A MS A is At Mezz. Encl 5812, MIB: RIA □, EHI A □ and RIA#1 □ are At encl 5813, M-1CB, RIA □ and encl 5814, M-2CB, RIA □ are Mod1 □ and Mod2 □ are High Voltage to Mod1 □ and Mod2 □ are Low Voltage to Mod1 □ and Mod2 □ are Attempt to turn on Low Voltage to Mod1 □ and Mod2 □ Attempt to turn on High Voltage to Mod1 □ and Mod2 □	OPEN OFF OFF ENABLED OFF OFF OFF FAIL FAIL
CLOSE VERIFY VERIFY RESET VERIFY VERIFY TURN ON VERIFY TURN ON VERIFY	MS A At Mezz. Encl 5812, MIB: RIA □, EHI A □ and RIA#1 □ are At encl 5813, M-1CB, RIA □ and encl 5814, M-2CB, RIA □ are RIA at encl 5813 and encl 5815 RIA Attempt to Enable On Mod1 □ and Mod2 □ Low Voltage to Mod1and Mod2 Low Voltage to Mod1 □ and Mod2 □ are High Voltage to Mod1 □ and Mod2 High Voltage to Mod1 □ and Mod2 □ are	ON ON RESET SUCCESSFUL ON ON
OPEN VERIFY VERIFY VERIFY VERIFY	MS B MS B is At Mezz. Encl 5812, MIB: RIB □, EHI B □ and RIB#2 □ are At encl 5813, M-1CB, RIB □ and encl 5814, M-2CB, RIB □ are At encl 5813 RIA is Mod1 □ and Mod2 □ are	OPEN OFF OFF ON ENABLED OFF
VERIFY VERIFY VERIFY VERIFY	High Voltage to Mod1 □ and Mod2 □ are Low Voltage to Mod1 □ and Mod2 □ are Attempt to turn on Low Voltage to Mod1 □ and Mod2 □ Attempt to turn on High Voltage to Mod1 □ and Mod2 □	OFF OFF FAIL FAIL
CLOSE VERIFY VERIFY VERIFY TURN ON VERIFY TURN ON VERIFY	MS B At Mezz. Encl 5812, MIB: RIB □, EHI B □ and RIB#2 □ are At encl 5813, M-1CB, RIB □ and encl 5814, M-2CB, RIB □ are Attempt to Enable On Mod1 □ and Mod2 □ Low Voltage to Mod1and Mod2 Low Voltage to Mod1 □ and Mod2 □ are High Voltage to Mod1 □ and Mod2 High Voltage to Mod1 □ and Mod2 □ are	ON ON SUCCESSFUL ON ON
PRESS	ES in ACR	
VERIFY VERIFY VERIFY VERIFY VERIFY VERIFY VERIFY	At Mezz. Encl 5812, MIB: RIA □, EHI A □ and RIA#1 □ are At Mezz. Encl 5812, MIB: RIB □, EHI B □ and RIB#2 □ are At encl 5813, M-1CB, RIA □ and encl 5814, M-2CB, RIA □ are At encl 5813, M-1CB, RIB □ and encl 5814, M-2CB, RIB □ are BS Mod1 □ and Mod2 □ are High Voltage to Mod1 □ and Mod2 □ are Low Voltage to Mod1 □ and Mod2 □ are	OFF OFF OFF CLOSED ENABLED OFF OFF

	VERIFY VERIFY	Attempt to turn on Low Voltage to Mod1 □ and Mod2 □ Attempt to turn on High Voltage to Mod1 □ and Mod2 □	FAIL FAIL
	RESET VERIFY RESET	ES in ACR ES in ACR is RIA at encl 5809 with SOR key	RESET
	VERIFY	RIA at encl 5809 is	RESET
	VERIFY	At Mezz. Encl 5812, MIB: RIA □, EHI A □ and RIA#1 □ are	ON
	VERIFY	At encl 5813, M-1CB, RIA □ and encl 5814, M-2CB, RIA □ are	ON
	RESET	RIB at encl 5809 with SOR key and Test RIB RIB at encl 5809 is	DECET
	VERIFY VERIFY	At Mezz. Encl 5812 , MIB : RIB \square , EHI B \square and RIB#2 \square are	RESET ON
	VERIFY	At encl 5813, M-1CB, RIB \square and encl 5814, M-2CB, RIB \square are	ON
	VERIFY	Attempt to Enable On Mod1 \(\) and Mod2 \(\)	SUCCESSFUL
		•	
	DISABLE VERIFY	Mod1 □ and Mod2 □	ENABLED OFF
	VERIF 1	Mod1 □ and Mod2 □ are	ENABLED OFF
	Pulsing	acceptance of Test interlocks will turn off Modulators while Ena	
		END OF TEST PROCEDURE	
TTL: Sion	n for completic	on of initial testing:	
TIL. Digi	rior compicate	in or initial testing.	 -
		Date: /_	/
TTL: Sign	n for completi	on of final testing:	
		Date: /_	/